Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Presently Amended) A bridge apparatus for connecting a first multimaster bus I^2C environment to a second multimaster bus I^2C environment, comprising:

an address bitmap having a value associated with each possible I^2C address;

a port-A interface that is connected to, and receives address signals and data signals from, the first multimaster bus, buffers the received address signals and data signals and ~~retransmits~~ generates new data signals ~~received from the second multimaster bus to~~ on the first multimaster bus;

a port-B interface independent from the port-A interface that ~~retransmits~~ is connected to, and generates new address signals and data signals ~~to~~ on, the second multimaster bus and receives data signals from the second multimaster bus; and

a controller that is connected to the port-A interface and to the port-B interface and responds to ~~an~~ buffered address and data received in the port-A interface from the first multimaster bus by controlling the port-B interface to selectively ~~retransmit~~ generate on the second multimaster bus new address and data signals corresponding to the received address and data depending on the address bitmap value associated with the received address.

2. (Original) The bridge apparatus of claim 1 wherein the controller comprises a command interpreter that receives commands at the port-A interface from the first multimaster bus and controls the operation of the bridge apparatus in response to received commands.

3. (Presently Amended) The bridge apparatus of claim 2 wherein a tunnel command received by the bridge apparatus includes a tunnel address and the controller ~~passes~~ responds to the tunnel address ~~to~~ by controlling the port-B interface ~~for transmission~~ to generate the tunnel address on the second multimaster bus.

4. (Original) The bridge apparatus of claim 2 further comprising a plurality of registers, each holding a value that control the operation of the bridge apparatus and wherein the command interpreter receives commands at the port-A interface from the first multimaster bus and places a value in at least one of the registers in response thereto.

5. (Original) The bridge apparatus of claim 4 wherein a first register holds a bridge ID value and each command contains a bridge ID value and wherein the command interpreter comprises a mechanism which responds to a command when the bridge ID value therein equals the bridge ID in the first register.

6. (Previously Amended) The bridge apparatus of claim 5 wherein a second register defines a range of bridge IDs and wherein the command interpreter comprises another mechanism that transmits a command received from the first multimaster bus on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

7. (Original) The bridge apparatus of claim 1 wherein the controller is a programmed microcontroller.

8. (Previously Amended) The bridge apparatus of claim 7 wherein the microcontroller comprises a RAM memory wherein the address bitmap is located.

9. (Original) The bridge apparatus of claim 7 wherein the microcontroller is connected to the port-A interface by a clock and data line and the microcontroller detects a START signal by generating an interrupt based on a signal on the data line.

10. (Presently Amended) A bi-directional bridge apparatus for connecting a first multimaster bus I^2C environment and a second multimaster bus I^2C environment, comprising:

a first unidirectional bridge device having, a first address bitmap with a value associated with each possible I^2C address, a first port-A interface that is connected to, and receives and buffers address and data signals from, the first multimaster bus, a first port-B interface independent from the first port-A interface that is ~~selectively responsive to address and data signals received on the first port-A interface in order to retransmit the~~ connected to, and generates new address and data signals ~~to~~ on the second multimaster bus; and a first controller that ~~selectively passes an~~ is connected to the first port-A interface and to the first port-B interface and is responsive to buffered address and data received on the first port-A interface from the first multimaster bus ~~to~~ for controlling the first port-B interface ~~for retransmission~~ to generate on the second multimaster bus new address and data corresponding to address and data received on the first multimaster bus depending on a first address bitmap value associated with the address received on the first port-A interface and

a second unidirectional bridge device having, a second address bitmap with a value associated with each possible I^2C address, a second port-A interface that is connected to, and receives and buffers address and data signals from the second multimaster bus, a second port-B interface independent from the second port-A interface that is ~~selectively responsive to address and data signals received on the second port-A interface in order to retransmit the~~ connected to, and generates new address and data signals ~~to~~ on the first multimaster bus[[;]], and a second controller that ~~selectively passes an~~ is connected to the second

port-A interface and the second port-B interface and is responsive to buffered address and data received on the second port-A interface from the second multimaster bus ~~to~~ for controlling the second port-B interface ~~for retransmission~~ to generate on the first multimaster bus new address and data corresponding to the address and data received on the second multimaster bus depending on a second address bitmap value associated with the address received on the second port-A interface.

11. (Previously Amended) The bi-directional bridge apparatus of claim 10 wherein each of the first and second unidirectional bridge devices comprises a mechanism for designating whether that unidirectional bridge device will have priority when both the first and second unidirectional bridge devices simultaneously begin a transaction.

12. (Previously Amended) The bi-directional bridge apparatus of claim 11 wherein each of the first and second unidirectional bridge devices further comprises a deadlock mechanism that cooperates with the designating mechanism and the deadlock mechanism of the other unidirectional bridge device for enabling one of the first and second unidirectional bridge devices and disabling the other unidirectional bridge device when both unidirectional bridge devices simultaneously begin a transaction.

13. (Previously Amended) The bi-directional bridge apparatus of claim 10 wherein the first unidirectional bridge device further comprises a plurality of registers, each holding a value that controls the operation of the first unidirectional bridge device and wherein the first controller comprises a first command interpreter that receives commands at the first port-A interface from the first multimaster bus and places a value in at least one of the registers in response thereto.

14. (Previously Amended) The bi-directional bridge apparatus of claim 13 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein the first command interpreter comprises a mechanism that transmits a command received from the first multimaster bus on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

15. (Previously Amended) The bi-directional bridge apparatus of claim 10 wherein the second unidirectional bridge device further comprises a plurality of registers, each holding a value that controls the operation of the second unidirectional bridge device and wherein the second controller comprises a second command interpreter that receives commands at the second port-A interface from the second multimaster bus and places a value in at least one of the registers in response thereto.

16. (Previously Amended) The bi-directional bridge apparatus of claim 15 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein the second command interpreter comprises a mechanism that transmits a command received from the second multimaster bus on the first multimaster bus when the bridge ID in the received command is outside the range of bridge IDs.

17. (Previously Amended) The bi-directional bridge apparatus of claim 15 wherein a first register in the first unidirectional bridge device holds a first bridge ID value and a second register in the second unidirectional bridge device holds a second bridge ID value different from the first bridge ID value.

18. (Previously Amended) The bi-directional bridge apparatus of claim 39 wherein each command contains a bridge ID value and wherein the first command

interpreter comprises a mechanism which responds to a command when the bridge ID value therein equals the first bridge ID.

19. (Previously Amended) The bi-directional bridge apparatus of claim 17 wherein each command contains a bridge ID value and wherein the second command interpreter comprises a mechanism which responds to a command when the bridge ID value therein equals the second bridge ID.

20. (Presently Amended) A method for connecting a first multimaster bus I^2C environment to a second multimaster bus I^2C environment, comprising

(a) connecting the first multimaster bus to the second multimaster bus with a bridge having an address bitmap with a value associated with each possible I^2C address, a port-A interface that is connected to, and receives address signals and data signals from the first multimaster bus, buffers the received address signals and data signals and ~~retransmits~~ generates new data signals ~~received from the second multimaster bus to~~ on the first multimaster bus and a port-B interface independent from the port-A interface that ~~retransmits~~ is connected to, and generates new address signals and data signals ~~to~~ on the second multimaster bus and receives data signals from the second multimaster bus; and

(b) in response to ~~an~~ buffered address and data received in the port-A interface from the first multimaster bus controlling the port-B interface to selectively ~~retransmit~~ generate new address and data on the second multimaster bus corresponding to the received address and data depending on the address bitmap value associated with the received address.

21. (Original) The method of claim 20 wherein step (b) comprises receiving commands at the port-A interface from the first multimaster bus and controlling the operation of the bridge apparatus in response to received commands.

22. (Original) The method of claim 21 wherein a tunnel command received by the bridge apparatus includes a tunnel address and wherein step (b) further comprises passing the tunnel address to the port-B interface for transmission on the second multimaster bus.

23. (Original) The method of claim 21 wherein the bridge further comprises a plurality of registers, each holding a value that control the operation of the bridge apparatus and wherein step (b) comprises receiving commands at the port-A interface from the first multimaster bus and places a value in at least one of the registers in response thereto.

24. (Original) The method of claim 23 wherein a first register holds a bridge ID value and each command contains a bridge ID value and wherein step (b) comprises responding to a command when the bridge ID value therein equals the bridge ID in the first register.

25. (Previously Amended) The method of claim 24 wherein a second register defines a range of bridge IDs and step (b) comprises transmitting a command received from the first multimaster bus on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

26. (Original) The method of claim 20 wherein the bridge comprises a programmed microcontroller that performs step (b).

27. (Previously Amended) The method of claim 26 wherein the microcontroller comprises a RAM memory wherein the address bitmap is located.

28. (Original) The method of claim 26 wherein the microcontroller is connected to the port-A interface by a clock and data line and the microcontroller detects a START signal by generating an interrupt based on a signal on the data line.

29. (Presently Amended) A method for connecting a first multimaster bus I^2C environment and a second multimaster bus I^2C environment, comprising

(a) connecting the first multimaster bus to the second multimaster bus with a first unidirectional bridge device having, a first address bitmap having a value associated with each possible I^2C address, a first port-A interface that is connected to, and receives address and data signals from the first multimaster bus, a first port-B interface independent from the first port-A interface that ~~transmits~~ is connected to, and generates new address and data signals ~~to~~ on the second multimaster bus;

(b) ~~selectively passing~~ in response to an address and data received on the port-A interface from the first multimaster bus ~~to~~ selectively controlling the first port-B interface ~~for transmission~~ to generate on the second multimaster bus new address and data corresponding to the address and data received from the first multimaster bus depending on the first address bitmap value associated with the address;

(c) connecting the second multimaster bus to the first multimaster bus with a second unidirectional bridge device having, a second address bitmap having a value associated with each possible I^2C address, a second port-A interface that is connected to, and receives address and data signals from the second multimaster bus, a second port-B interface independent from the second port-A interface that ~~transmits~~ is connected to, and generates new address and data signals ~~to~~ on the first multimaster bus; and

(d) ~~selectively passing~~ in response to an address and data received on the port-A interface from the second multimaster bus ~~to~~ selectively controlling the second port-B interface ~~for transmission~~ to generate on the first

multimaster bus new address and data corresponding to the address and data received from the second multimaster bus depending on the second address bitmap value associated with the address.

30. (Original) The method of claim 29 wherein both the first and second unidirectional bridge devices have a mechanism for designating whether a unidirectional bridge device is one of an upstream bridge and a downstream bridge.

31. (Original) The method of claim 29 further comprising a deadlock mechanism for choosing one of the unidirectional bridge devices when both unidirectional bridge devices simultaneously begin a transaction.

32. (Original) The method of claim 29 wherein the first unidirectional bridge device further comprises a plurality of registers, each holding a value that control the operation of the first unidirectional bridge device and wherein step (b) comprises receiving commands at the port-A interface from the first multimaster bus and placing a value in at least one of the registers in response thereto.

33. (Original) The method of claim 32 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein step (b) comprises transmitting a received command on the second multimaster bus when the bridge ID in the received command is in the range of bridge IDs.

34. (Original) The method of claim 29 wherein the second unidirectional bridge device further comprises a plurality of registers, each holding a value that control the operation of the second unidirectional bridge device and wherein step (d) comprises receiving commands at the port-A interface from the second

multimaster bus and placing a value in at least one of the registers in response thereto.

35. (Original) The method of claim 34 wherein each of the commands contains a bridge ID and at least one of the registers defines a range of bridge IDs and wherein step (d) comprises transmitting a received command on the first multimaster bus when the bridge ID in the received command is outside the range of bridge IDs.

36. (Original) The method of claim 34 wherein a register in the first unidirectional bridge device holds a first bridge ID value and a register in the second unidirectional bridge device holds a second bridge value different from the first bridge ID value.

37. (Original) The method of claim 36 wherein each command contains a bridge ID value and wherein step (b) comprises responding to a command when the bridge ID value therein equals the bridge ID in the first register.

38. (Original) The method of claim 37 wherein each command contains a bridge ID value and wherein step (d) comprises responding to a command when the bridge ID value therein equals the bridge ID in the first register.

39. (Previously Added) The bi-directional bridge apparatus of claim 13 wherein a register in the first unidirectional bridge device holds a first bridge ID value and a register in the second unidirectional bridge device holds a second bridge ID value different from the first bridge ID value.